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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,291	06/07/2001	David F. Tobias	1001-0179	9539

22120 7590 03/01/2006

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,291	TOBIAS ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 have been presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 29-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the specification does explicitly teach state throttling is not used in any of the performance states.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-2, 4-11, 13-24 and 26-28 are rejected under 35 U.S.C. 102(a) as anticipated by Cooper et al [Cooper] US Pat No 6829713.

6. Referring to claim 1, Cooper teaches the invention substantially including:

   a. determining utilization of an integrated circuit (IC) [fig. 6, col. 7 lines 3-10].

b. comparing the determined utilization to a threshold utilization value [fig. 6, col. 7 lines 3-34].

c. if the determined utilization is above the threshold utilization value, entering a higher predetermined performance state as the next performance state [fig. 6, col. 7 lines 3-34].

In particular, Cooper explicitly teaches comparing CPU utilization to a utilization threshold and entering the performance state associated with that threshold. Therefore, if the CPU was operating in one of the two battery optimized modes (battery optimized with and without clock throttling) and the CPU utilization spiked to over 95%, the system would *always* enter the maximum performance mode (610). For example, if the CPU utilization in Cooper is less than 20% and is in a battery optimized mode without clock throttling (618, 620) and the CPU utilization spikes to over 95%, Cooper would immediately enter the maximum performance state (610), skipping the battery optimized mode with clock throttling (614, 616).

7. Referring to claim 2, Cooper teaches the predetermined performance state being a maximum performance as seen in the above argument.

8. Referring to claims 4 and 5, Cooper teaches a plurality of power modes which entered according to CPU utilization [fig. 6].

9. Referring to claims 6 and 7, Cooper teaches adjusting voltage and frequency [col. 1 lines 27-33].

10. Referring to claim 8, Cooper teaches determining the utilization periodically [col. 5 lines 38-39].

11. Referring to claim 9, Cooper teaches the integrated circuit includes a CPU [fig. 6].

12. Referring to claim 10, this is rejected on the same basis as set forth hereinabove. In addition, the Cooper system requires that the CPU enter a maximum performance mode whenever the CPU utilization is above the 95% threshold. Therefore it is interpreted that every time the CPU utilization exceeds the 95% threshold mark, the CPU will enter the same maximum performance mode.

13. Referring to claim 11, this is rejected on the same basis as set forth hereinabove. In addition, Cooper teaches that the system may comprise instructions to perform the above methods [col. 3 line 66 – col. 4 line 5].

14. Referring to claims 13-23 and 26-28, these are rejected on the same basis as set forth hereinabove. Cooper teaches the method and therefore teaches the system performing the method. In addition, Cooper also teaches instructions for performing the method [col. 3 line 66 – col. 4 line 5].

15. Referring to claim 24, Hetzler teaches that the computer readable medium can come from many different sources [col. 25 lines 54-58].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3, 12, 25 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper as applied to claims 1-2, 4-11, 13-24 and 26-28 above.

18. Referring to claim 3, although Cooper teaches a plurality of performance states end entering one of the performance states based on whether a utilization threshold has been crossed, the only way Cooper skips any of the performance states is when the system transitions from a battery optimized mode without clock throttling to maximum performance mode. Through this particular transition, a battery optimized mode with clock throttling can be skipped. Whenever the system transitions to the battery optimized mode with clock throttling (interpreted as a near maximum performance state) no performance states are skipped because Cooper does not have any intermediate performance states between the near maximum performance state and its battery optimized mode without clock throttling and therefore does not skip any performance states when transitioning to the near maximum performance state. In particular, this is due to the fact that Cooper only teaches three performance states. Systems which comprise more than three performance states are well known in the art and it would have been obvious to modify Cooper to include additional performance states because the more performance states a CPU has the more optimally the CPU can operate in accordance with a particular CPU utilization. In addition, it is interpreted that additional threshold values would be used to indicate which performance mode should be entered as was done in the original Cooper system. Subsequently, it is interpreted that if a utilization value indicates that a CPU should enter a near maximum performance mode, the CPU would immediately enter that mode and skip any intermediate performance mode between the CPUs previous performance mode and the near maximum performance mode as was originally taught by Cooper argued above.

19. Referring to claims 12 and 25, these are rejected on the same basis as set forth hereinabove.

20. Referring to claims 29-32, Cooper teaches that rather than throttling a clock signal to reduce power consumption, lower frequency clock signals can be generated independently or derived from an existing clock [col. 1 lines 42-52]. It is obvious that any of the above clocking techniques could be applied to the Cooper system as they all provide the same benefit of reducing power.

Response to Arguments

21. Applicant's arguments filed 1/25/06 have been fully considered but they are not persuasive.

22. Applicants argue in substance that Cooper does not teach or suggest always skipping at least one intermediate performance state that is between a current performance state and a predetermined performance state nor does Cooper teach or suggest skipping an intermediate performance state that has a greater associated integrated circuit utilization than a current performance state.

23. In response to applicant's argument, applicant believes that "a 'maximum battery mode,' is a lower CPU performance state than the battery optimized mode (w/o signal throttling)." It is believed by the examiner that the rationale behind applicants belief is that in a maximum performance mode, there is no clock throttling and therefore it would appear that any kind of throttling would only reduce performance. Therefore, it is believed by applicant that a battery optimized mode (w/o throttling) otherwise referred to as a "maximum battery mode" actually has a higher performance than the battery optimized mode (w/ throttling). Unfortunately, in this instance, the above interpretation is incorrect and rather the battery optimized mode (w/

throttling) actually is a higher performance mode than the "maximum battery mode" which will be proved below.

First of all, Cooper states that tasks are to be completed as quickly as possible so that the system can "transition after their completion to an even lower power state than can be achieved with clock throttling, conserving more overall power" [col. 6 line 66- col. 7 line 2]. This is evidence that even though the battery optimized mode (w/ throttling) involves throttling a clock, it does not necessarily mean that its performance mode is less than the performance of the battery optimized mode (w/o throttling). Also, Cooper explicitly states that the battery optimized mode (w/o throttling) comprise the C2 and C3 ACPI power states [col. 7 lines 19-30]. The examiner has supplied a portion of the ACPI specification to illustrate that the C2 and C3 power states are the lowest power states defined in ACPI. Therefore, if a battery optimized mode (w/o throttling) is equivalent to the C3 state, there is no possible way that the battery optimized mode (w/ throttling) could be a lower performance state because ACPI defines the C3 state as the *lowest* performance state. From these two examples alone it should be apparent that Cooper does teach that a battery optimized mode (w/o throttling) is a lower performance state than a battery optimized mode (w/o throttling).

In conclusion, if the current CPU utilization in Cooper is less than 20% and is in a battery optimized mode (w/o throttling) and the CPU utilization spikes to over 95%, Cooper would immediately enter the maximum performance state, skipping the battery optimized mode (w/ throttling) which has been proven as being an intermediate performance mode. In addition, it can be seen in fig. 6 in Cooper that an intermediate utilization (95% > utilization > 20%) is

greater than a current utilization (20% > utilization) when transitioning from a minimum performance state (20% > utilization) to a maximum performance state (utilization > 95%).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
February 16, 2006